21. (New) The bus system of claim 20, further comprising:

at least one state machine for controlling the at least one interface unit.

22. (New) The bus system of claim 21, wherein the at least one state machine controls an external bus.

23. (New) The bus system of claim 20, further comprising:

an address generator in communication with the processing unit, the address generator for generating an address for selecting a unit coupled to the bus system.

24. (New) The bus system of claim 20, further comprising:

a second plurality of lines coupled to the at least one interface unit, the second plurality of lines for at least one of reading data and writing data.

25. (New) The bus system of claim 20, further comprising:

at least one internal bus system coupled to the at least one interface unit, the at least one internal bus system including a plurality of individual lines, the at least one internal bus system for at least one of reading data and writing data.

26. (New) The bus system of claim 20, further comprising:

at least one register coupled to the plurality of lines for managing and controlling the bus system.

27. (New) The bus system of claim 20, the bus system further comprising:

a bus master unit coupled to the plurality of lines for controlling the bus system; and

a plurality of slave units in communication with the bus master unit.

28. (New) The bus system of claim 27, wherein control of the bus system is transferred dynamically from the bus master unit to another unit coupled to the bus system.

29. (New) The bus system of claim 28, wherein at least one of the plurality of slave units request control of the bus system.

30. (New) The bus system of claim 20, further comprising:

a register in communication with the at least one interface, the register indicating whether data is stored in the at least one interface.

31. (New) The bus system of claim 20, wherein the at least one interface is at least one of integral with the processing unit and formed by a configuration of at plurality of logic cells, each of the plurality of logic cells implementing simple logical functions according to a logic cell configuration.

32. (New) The bus system of claim 20, wherein the plurality of interfaces are configured by at least one of a primary logic unit and the processing unit.

33. (New) The bus system of claim 32, wherein the primarily logic unit is at least partially integrated with the processing unit.